



Docket No.: 300.1119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Masatoshi AKAGAWA, et al.

Serial No. 10/612,222

Group Art Unit: 3726

Confirmation No. 5751

Filed: July 3, 2003

Examiner: Rick Kiltae Chang

For: COMPONENT-EMBEDDED BOARD FABRICATION METHOD AND APPARATUS FOR
HIGH-PRECISION AND EASY FABRICATION OF COMPONENT-EMBEDDED BOARD
WITH ELECTRONIC COMPONENTS EMBEDDED IN WIRING BOARD

COMMUNICATION TO THE EXAMINER

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The following documents are submitted herewith with respect to the above-identified application:

Office Action mailed from the U.S. Patent and Trademark Office on October 6, 2008 in U.S. patent application serial no. 12/004,431;

Office Action mailed from the U.S. Patent and Trademark Office on May 13, 2009 in U.S. patent application serial no. 12/004,431;

Notice of Allowance and Fee(s) Due mailed from the U.S. Patent and Trademark Office on December 15, 2009 in U.S. patent application serial no. 12/004,431;

Office Action mailed from the U.S. Patent and Trademark Office on December 29, 2009 in U.S. patent application serial no. 12/004,431; and

U.S. Patent No. 6,407,929, cited by the Examiner of U.S. patent application serial no. 12/004,431 in the Office Action mailed on October 6, 2008.

Applicants respectfully request that the enclosed documents be placed into the application file.

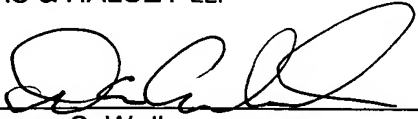
Serial No. 10/612,222

If there are any additional fees associated with filing of this Communication, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 8-6-10

By: 
Aaron C. Walker
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/004,431	12/21/2007	Masatoshi Akagawa	300.1119D	2110
21171 7590 10/06/2008 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER NGUYEN, DONGHAI D	
			ART UNIT 3729	PAPER NUMBER
			MAIL DATE 10/06/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



Office Action Summary	Application No. 12404,431	Applicant(s) AKAGAWA ET AL.
	Examiner DONGHAI D. NGUYEN	Art Unit 3729

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2008.
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
4a) Of the above claim(s) 2-5 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 21 December 2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>12/21/07; 5/30/08</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claim 1, in the reply filed on August 11, 2008 is acknowledged. Thus, claims 2-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

Drawings

2. Figures 19 and 20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is too long. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --A COMPONENT-EMBEDDED CIRCUIT BOARD FABRICATION METHOD--.

Note: the Abstract also needs to be modified to read on the elected claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,386,623 to Okamoto et al in view of US Patent 6,407,929 to Hale et al.

Okamoto et al disclose a component-embedded board fabrication method for fabricating a component-embedded board (1) with electronic components (3) embedded within a wiring board (1), comprising: detecting, before said board is covered with a first insulating layer, the actual position of a first electronic component (3) formed on a surface of said board (1, see Col. 11, lines 1-12); calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data (see Col. 11, line 13-27); correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component (see Col. 12, lines 7-19); forming via holes (9) in the first insulating layer in accordance with the corrected design data, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer (Col. 12, lines 29-36); and using the step of detecting calculating, correcting and forming via holes to build up the component-

Art Unit: 3729

embedded board (see Fig. 1 and Col. 9, line 64 to Col. 10, line 4). However, Okamoto et al do not disclose the second electronic component formed on a surface of the first insulating layer. Hale et al teach the method of fabricating a component-embedded board having the second electronic component (1106) formed on a surface of the first insulating layer (1104) for forming multi-level of electronic package using build-up process. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Okamoto et al by utilized the fabrication of multi-level of electronic package using build-up process as taught by Hale et al for obtaining a desired component-embedded board. Note that the detecting step is executed before the insulation layer covers the board because the position marks (M) on the chip (3) must be exposed to reflect light from the detector (see Col. 11, lines 7-12).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art references cited for their teachings of fabricating component-embedded board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONGHAI D. NGUYEN whose telephone number is (571)272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

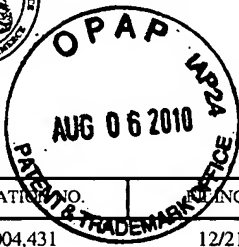
DN
October 1, 2008

/Donghai D. Nguyen/
Primary Examiner, Art Unit 3729



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/004,431	12/21/2007	Masatoshi Akagawa	300.1119D	2110

21171 7590 05/13/2009
STAAS & HALSEY LLP
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1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

NGUYEN, DONGHAI D

ART UNIT	PAPER NUMBER
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3729

MAIL DATE	DELIVERY MODE
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05/13/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/004,431	Applicant(s) AKAGAWA ET AL.	
	Examiner DONGHAI D. NGUYEN	Art Unit 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) 2-5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 February 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
- 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
- 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

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Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3/26/09</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed on February 4, 2009 has been considered and made of record.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. the limitations: "detecting, before said board is covered with a first insulating layer, actual positions of terminals of a first electronic component formed on a surface of said board" (claim 1, lines 4-5) was not described in the specification at the time the application was filed. as best page 13, lines 4-7 describes a connecting terminal position of an electronic component is read from the captured image data but not a plurality of terminals is detected as currently claimed.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is vague and indefinite because it contains certain limitations that not disclosed in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 1, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,386,623 to Okamoto et al in view of US Patent 6,407,929 to Hale et al.

Okamoto et al disclose a component-embedded board fabrication method for fabricating a component-embedded board (1) with electronic components (3) embedded within a wiring board (1), comprising: detecting, before said board is covered with a first insulating layer, the actual position of a first electronic component (3) formed on a surface of said board (1, see Col. 11, lines 1-12); calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data (see Col. 11, line 13-27); correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component (see Col. 12, lines 7-19); forming via holes (9) in the first insulating layer in accordance with the corrected design data, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer (Col. 12, lines 29-36); and using the

step of detecting calculating, correcting and forming via holes to build up the component-embedded board (see Fig. 1 and Col. 9, line 64 to Col. 10, line 4). However, Okamoto et al do not disclose the second electronic component formed on a surface of the first insulating layer. Hale et al teach the method of fabricating a component-embedded board having the second electronic component (1106) formed on a surface of the first insulating layer (1104) for forming multi-level of electronic package using build-up process. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Okamoto et al by utilized the fabrication of multi-level of electronic package using build-up process as taught by Hale et al for obtaining a desired component-embedded board. Note that the detecting step is executed before the insulation layer covers the board because the position marks (M) on the chip (3) must be exposed to reflect light from the detector (see Col. 11, lines 7-12).

Also, Okamoto et al does not detecting actual positions of terminals of a first electronic component. It would have been an obvious matter of design choice to one having ordinary skill in the art at the time the invention was made to choose any desired method of detecting the position of the electronic component on the substrate such as by detecting positions of terminals of a first electronic component, since Applicants have not disclosed the specifics method of detecting actual positions of terminals of a first electronic component, solves any stated problem or for any particular purposes and it appears that the invention would perform equally well with the method of detecting actual position of the electronic component by detecting actual positions of alignment marks (68) of a first electronic component as disclosed by Okamoto et al (see Col. 9, lines 1-36).

Response to Arguments

8. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

The newly amended subject matter to claim 1 raises new issue as rejected above (see paragraphs 3-5).

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "a bending point") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONGHAI D. NGUYEN whose telephone number is (571)272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derris H. Banks can be reached on (571)-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN
May 11, 2009

/Donghai D. Nguyen/
Primary Examiner, Art Unit 3729



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

21171

12/15/2009

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

NGUYEN, DONGHAI D

ART UNIT

PAPER NUMBER

3729

DATE MAILED: 12/15/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/004,431

12/21/2007

Masatoshi Akagawa

300.1119D

2110

TITLE OF INVENTION: A COMPONENT-EMBEDDED CIRCUIT BOARD FABRICATION METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/15/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B-1 FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

21171 7590 12/15/2009

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Certificate of Mailing or Transmission

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/004,431 12/21/2007 Masatoshi Akagawa 300.1119D 2110

TITLE OF INVENTION: A COMPONENT-EMBEDDED CIRCUIT BOARD FABRICATION METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$300 \$0 \$1810 03/15/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
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NGUYEN, DONGHAI D 3729 029-852000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/004,431	12/21/2007	Masatoshi Akagawa	300.1119D	2110
21171	7590	12/15/2009		
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005				
			EXAMINER NGUYEN, DONGHAI D	
			ART UNIT	PAPER NUMBER
			3729	
DATE MAILED: 12/15/2009				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/004,431	AKAGAWA ET AL.	
	Examiner	Art Unit	
	DONGHAI D. NGUYEN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to an Amendment filed on August 13, 2009.
2. ☒ The allowed claim(s) is/are 1-4.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>8/13/09</u> 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input checked="" type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date <u>herein</u>. 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____. |
|---|--|

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 13, 2009 has been entered.

Election/Restrictions

2. Claim 1 is allowable. The restriction requirement between Groups I-V, as set forth in the Office action mailed on July 25, 2008, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claims 2-4, directed to Inventions II-IV are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim. However, claim 5, directed to Invention V stands withdrawn from consideration because it does not require all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with JOHN R. BEDNARZ on October 26, 2009.

The application has been amended as follows:

In the Claims:

Claims 1-4 has been changed as show below, added text with underlining and deleted text with strikethrough.

1. A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:
detecting, before said board is covered with a first insulating layer, actual positions of terminals of a first electronic component formed on a surface of said board;

Art Unit: 3729

calculating a set of displacements between design positions of terminals of said first electronic component and the actual positions of the terminals of said first electronic component on the surface of said board, and holding said set of displacements as first displacement data;

correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component;

forming via holes in the first insulating layer in accordance with the corrected design data, thereby compensating for an actual location of the displaced first electronic component in a subsequent layer; detecting, before said board is covered with a second insulating layer, actual positions of terminals of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded in the first insulating layer;

calculating a set of displacements between design position of terminals of said second electronic component and the actual position of the terminals of said second electronic component on the surface of said first insulating layer, and holding said set of displacements as second displacement data; and

correcting, based on said second displacement data, design data to be used for processing said board the processing including one of creating a bending point to reroute a wiring line, increasing the wiring line, and decreasing the wiring line after said board is covered with said second insulating layer; and

applying a maskless exposure onto the first and second insulating layers of the board based on the corrected design data for forming the wiring pattern and the wiring line.

2. A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

detecting, before said board is covered with a first insulating layer, ~~the~~ actual positions of a terminals of a first electronic component formed on a surface of said board;

calculating a set of displacements ~~displacement~~ between ~~the~~ design positions of terminals of said first electronic component and the actual positions the terminals of said first electronic component on the surface of said board, and holding said set of displacements ~~displacement~~ as first displacement data;

correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component;

forming via holes in the first insulating layer in accordance with the corrected design data, thereby compensating for ~~the~~ an actual location of the displaced first electronic component in a subsequent layer;

capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded in the first insulating layer;

calculating a displacement between a ~~the~~ design position of said second electronic component and ~~the~~ an actual position of said second electronic component detected from second image data obtained by imaging the surface of said first insulating layer, and holding said displacement as second displacement data; ~~and~~

correcting, based on said second displacement data, design data to be used for processing said board the processing including one of creating a bending point to reroute a wiring line, increasing the wiring line, and decreasing the wiring line after said board is covered with said second insulating layer; and

applying a maskless exposure onto the first and second insulating layers of the board based on the corrected design data for forming the wiring pattern and the wiring line.

3. A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

capturing, before said board is covered with a first insulating layer, an image of a surface of said board layer on which a first electronic component is formed;

calculating a displacement between ~~a~~ the design position of said first electronic component and ~~the~~ an actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data;

correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component;

forming via holes in the first insulating layer in accordance with the corrected design data, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer;

detecting, before said board is covered with a second insulating layer, ~~the actual positions~~ of terminals of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded in the first insulating layer;

calculating a set of displacements ~~displacement~~ between ~~the design positions of terminals~~ of said second electronic component and ~~the actual positions of the terminals~~ of said second electronic component on the surface of said first insulating layer, and holding said set of displacements ~~displacement~~ as second displacement data; ~~and~~

correcting, based on said second displacement data, design data to be used for processing said board the processing including one of creating a bending point to reroute a wiring line, increasing the wiring line, and decreasing the wiring line after said board is covered with said second insulating layer; and

applying a maskless exposure onto the first and second insulating layers of the board based on the corrected design data for forming the wiring pattern and the wiring line.

4. A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

capturing, before said board is covered with a first insulating layer, an image of a surface of said board on which a first electronic component is formed;

calculating a displacement between a ~~the~~ design position of said first electronic component and ~~the~~ an actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data;

correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component;

forming via holes in the first insulating layer in accordance with the corrected design data, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer;

capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded in the first insulating layer;

calculating a displacement between ~~a~~ the design position of said second electronic component and ~~the~~ an actual position of said second electronic component detected from second image data obtained by imaging the surface of said first insulating layer, and holding said displacement as second displacement data; ~~and~~

correcting, based on said second displacement data, design data to be used for processing said board the processing including one of creating a bending point to reroute a wiring line, increasing the wiring line, and decreasing the wiring line after said board is covered with said second insulating layer; and

applying a maskless exposure onto the first and second insulating layers of the board based on the corrected design data for forming the wiring pattern and the wiring line.

claim 5 has been canceled.

4. The following is an examiner's statement of reasons for allowance: prior art references fail to teach or suggest the method for fabricating a component embedded board includes: "detecting, calculating, and correcting the positions of the first and second components and then applying the maskless exposure to the first and second insulating layers of the board base on the corrected design data for forming the via holes and the wiring line on the board" in combination with other limitations as recited in details of claims 1-4.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONGHAI D. NGUYEN whose telephone number is (571)272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derris H. Banks can be reached on (571)-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN
October 26, 2009

/Donghai D. Nguyen/
Primary Examiner, Art Unit 3729



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/004,431	12/21/2007	Masatoshi Akagawa	300.1119D	2110
21171 7590 12/29/2009 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER NGUYEN, DONGHAI D	
			ART UNIT 3729	PAPER NUMBER
			MAIL DATE 12/29/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

**Supplemental
Notice of Allowability**

Application No.

12/004,431

Examiner

DONGHAI D. NGUYEN

Applicant(s)

AKAGAWA ET AL.

Art Unit

3729

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to IDS filed on 12/14/2009.
2. ☒ The allowed claim(s) is/are 1-4.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>12/14/09</u> | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____. |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 14, 2009 was filed before the mailing date of the Notice of Allowance on December 15, 2009. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance: the IDS filed on 12/14/2009 has been carefully reviewed and considered, but the patentability of the claims 1-4 is confirmed for the same reasons set for in the Notice of Allowance dated 12/15/2009.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONGHAI D. NGUYEN whose telephone number is (571)272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derris H. Banks can be reached on (571)-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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DN
December 22, 2009

/Donghai D. Nguyen/
Primary Examiner, Art Unit 3729



US006407929B1

(12) **United States Patent**
Hale et al.

(10) **Patent No.:** **US 6,407,929 B1**
(45) **Date of Patent:** **Jun. 18, 2002**

(54) **ELECTRONIC PACKAGE HAVING
EMBEDDED CAPACITORS AND METHOD
OF FABRICATION THEREFOR**

(75) **Inventors:** **Aaron Dean Hale, Chandler; Michael
Walk; David G. Figueroa**, both of
Mesa; **Joan K. Vrtis**, Phocnix, all of
AZ (US); **Toshimi Kohmura**,
Ibaraki-ken (JP)

(73) **Assignee:** **Intel Corporation, Santa Clara, CA
(US)**

(*) **Notice:** Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/606,882**

(22) **Filed:** **Jun. 29, 2000**

(51) **Int. Cl.⁷** **H05K 1/18**

(52) **U.S. Cl.** **361/763; 361/306.2; 361/760;
361/761; 361/782; 361/793; 257/724; 29/832**

(58) **Field of Search** **361/306.2, 734,
361/738, 761-764, 780, 782, 792, 793-795,
760; 174/255, 260; 257/691, 700-703,
723, 724, 728; 333/247; 29/832**

(56) **References Cited**

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4,349,862 A * 9/1982 Bajorek et al. 361/762
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ogy", *Electronic Circuits World Convention* 8, 6 p., (Sep. 8,
1999).

* cited by examiner

Primary Examiner—Kamand Cuneo

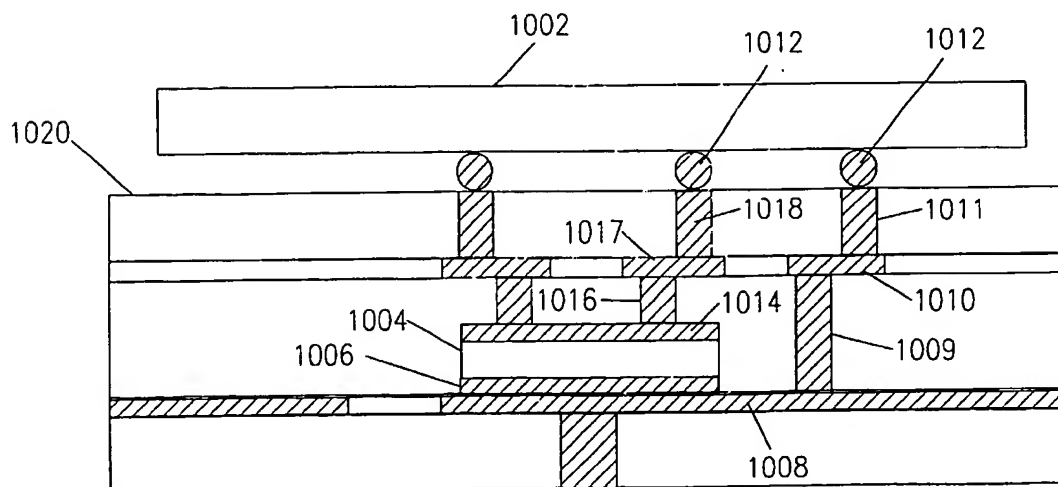
Assistant Examiner—John B. Vigushin

(74) *Attorney, Agent, or Firm*—Schwegman, Lundberg,
Woessner & Kluth, P.A.

(57) **ABSTRACT**

An electronic package (302, FIG. 3) includes one or more
capacitors (308) embedded within one or more layers (310)
of the package. The embedded capacitors are discrete
devices, such as integrated circuit capacitors (FIGS. 17-18)
or ceramic capacitors. During the package build-up process,
the capacitors are mounted (410, FIG. 4) to a package layer,
and a non-conductive layer is applied (412) over the capaci-
tors. When the build-up process is completed, the capaci-
tor's terminals (604, 608, FIG. 6) are electrically connected
to the top surface of the package. The embedded capacitor
structure can be used in an integrated circuit package (1904,
FIG. 19), an interposer (1906), and/or a printed circuit board
(1908).

29 Claims, 10 Drawing Sheets



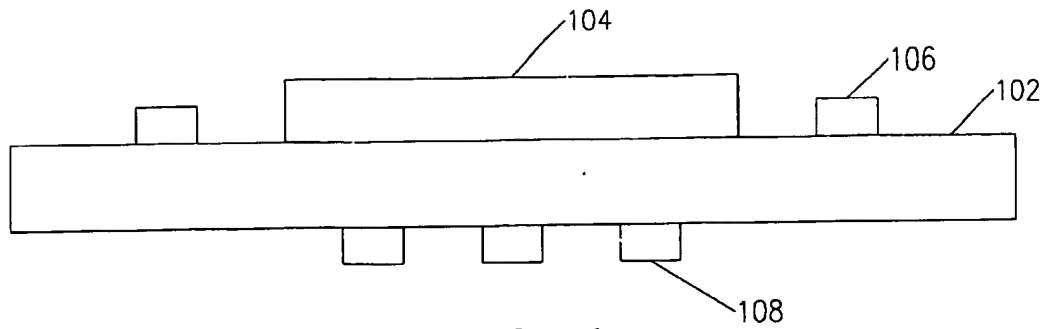


FIG. 1
(PRIOR ART)

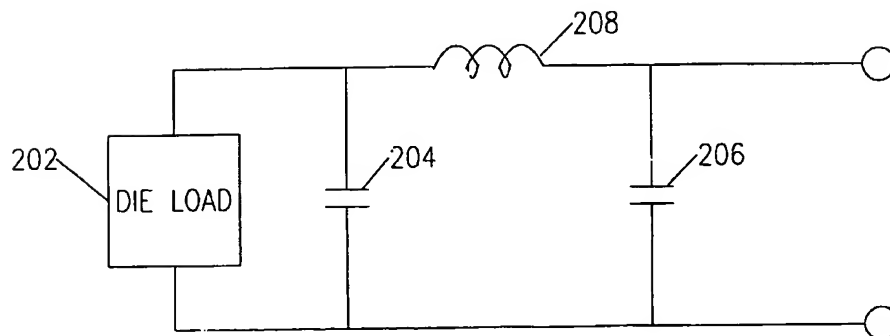
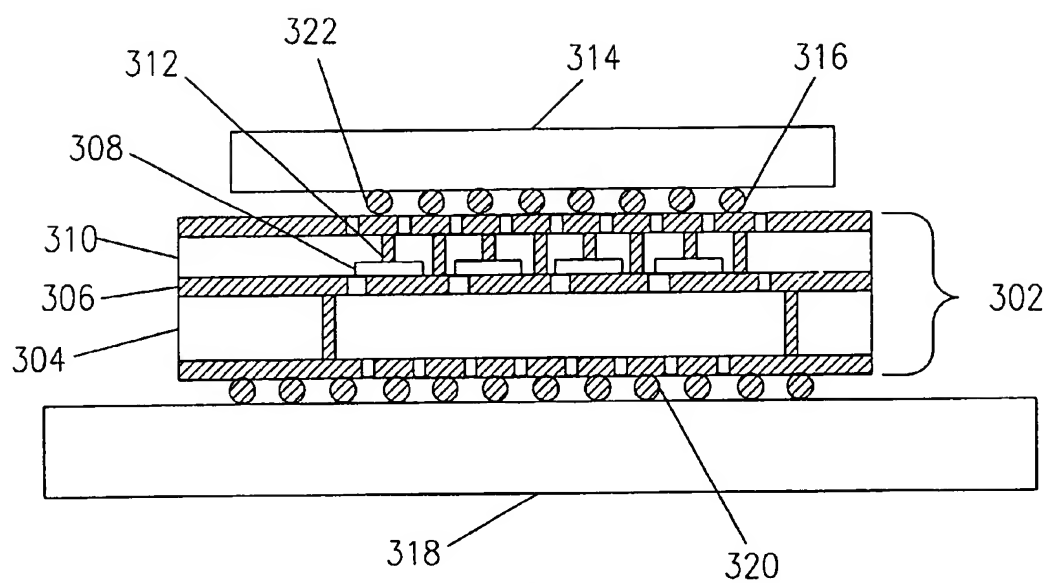
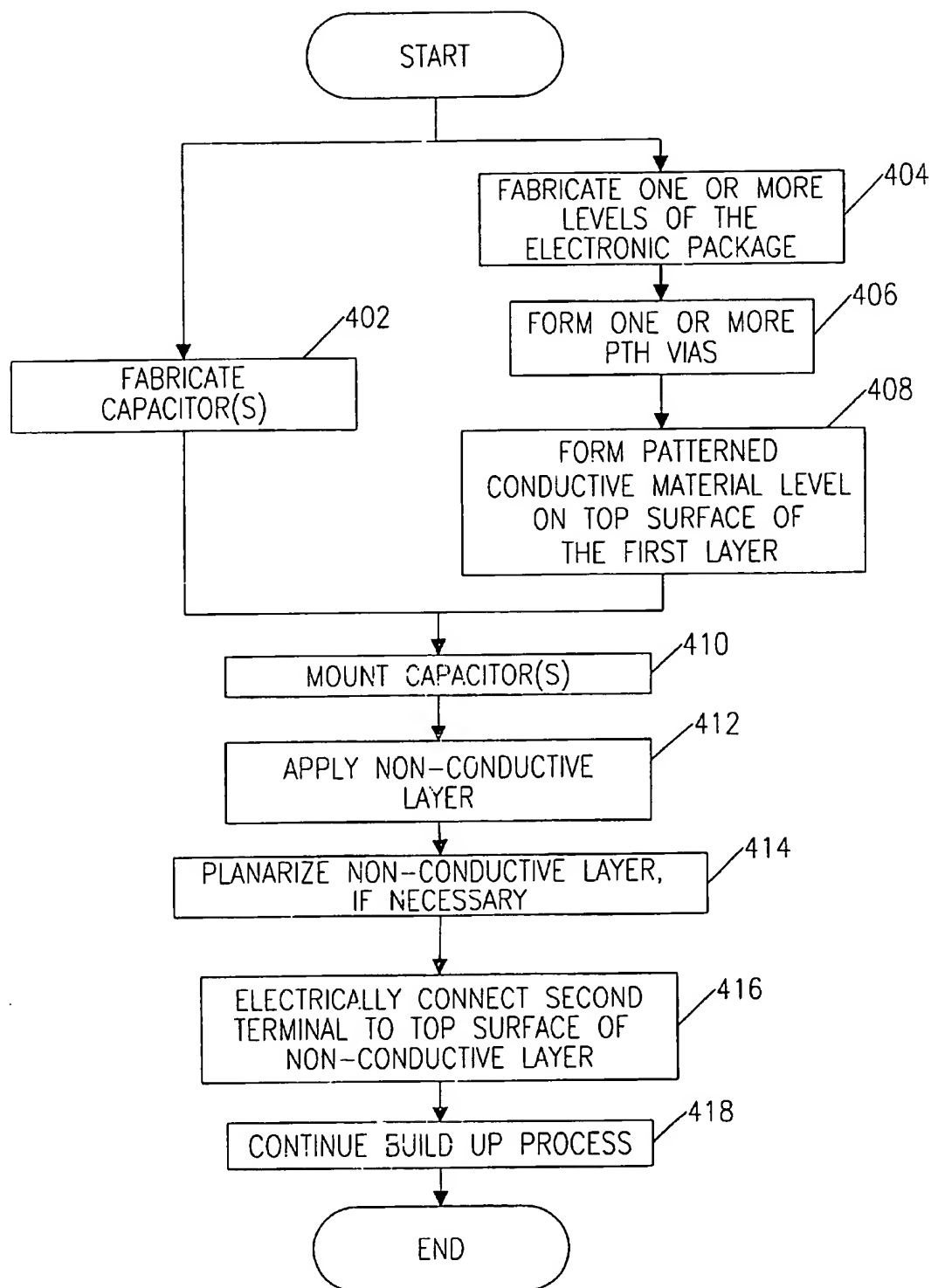


FIG. 2
(PRIOR ART)

**FIG. 3**

**FIG. 4**

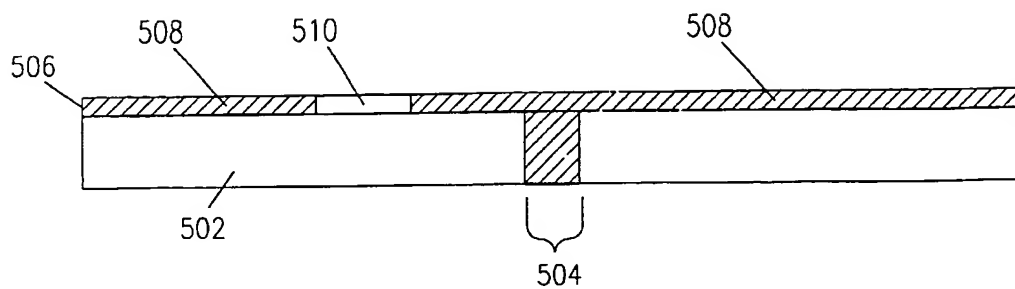


FIG. 5

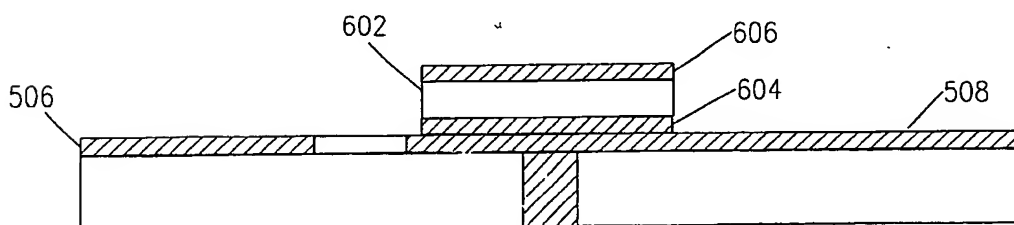


FIG. 6

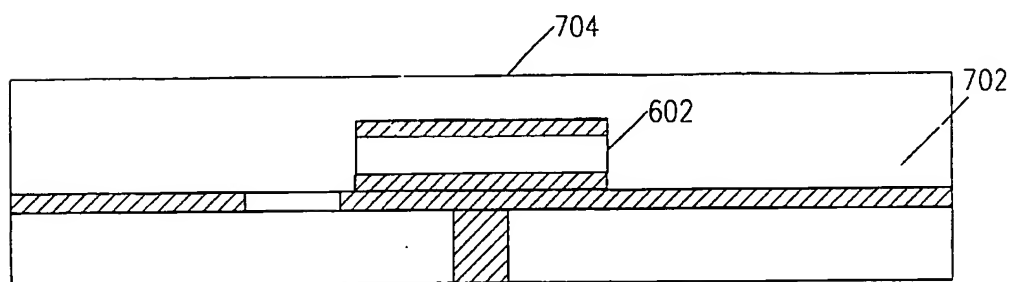


FIG. 7

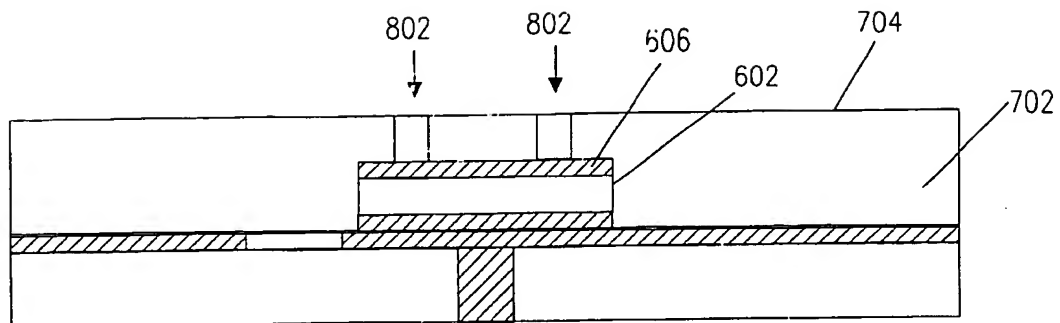


FIG. 8

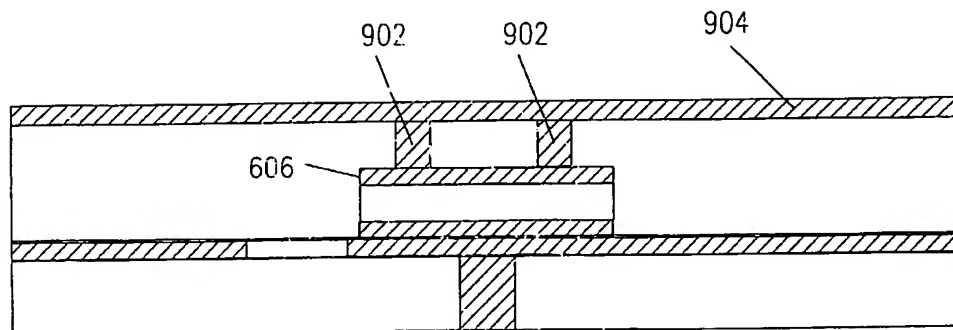


FIG. 9

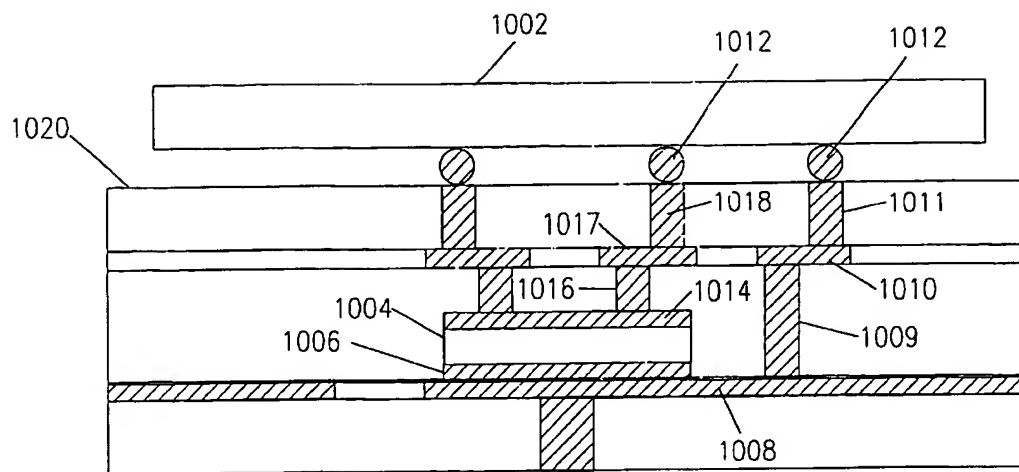


FIG. 10

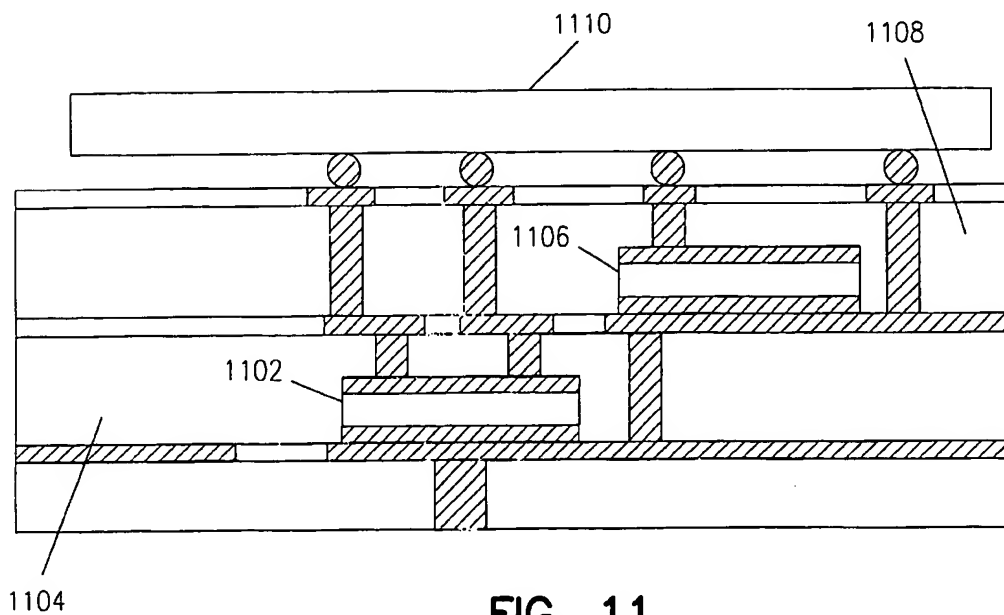


FIG. 11

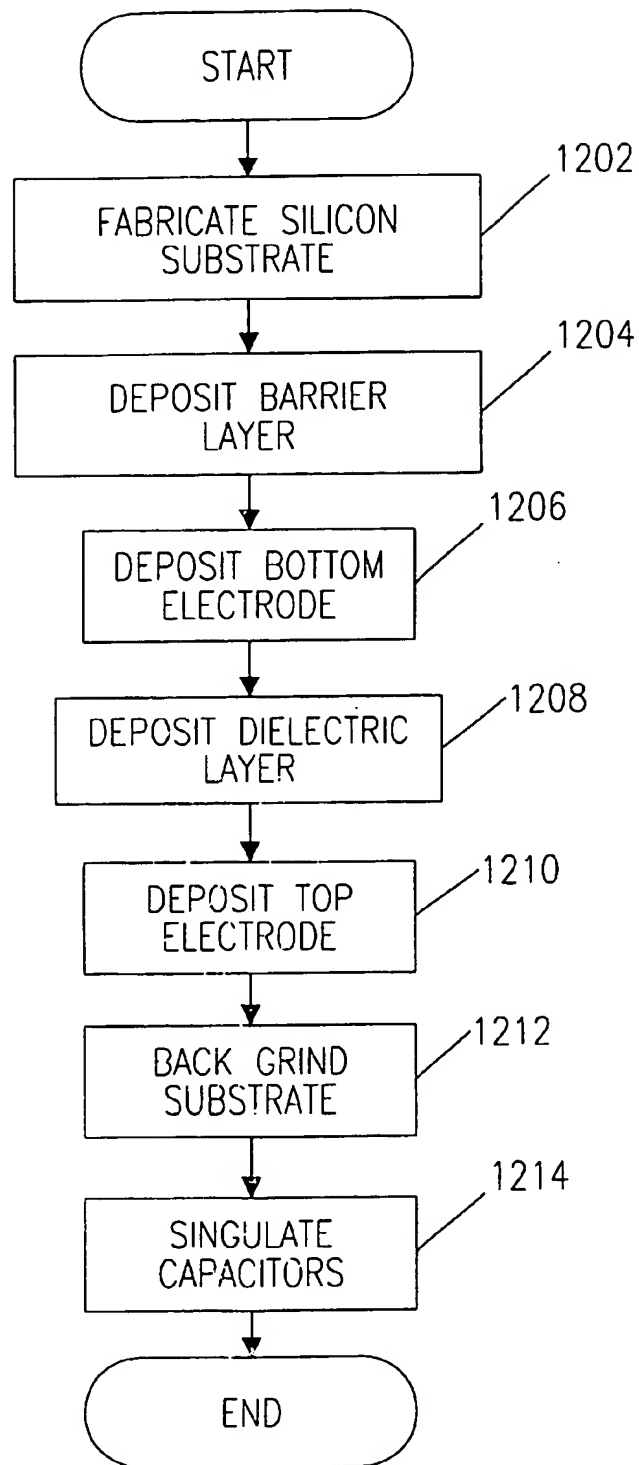
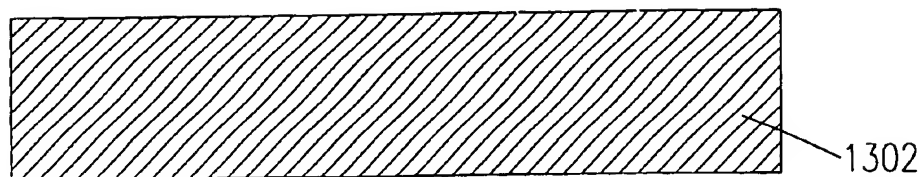
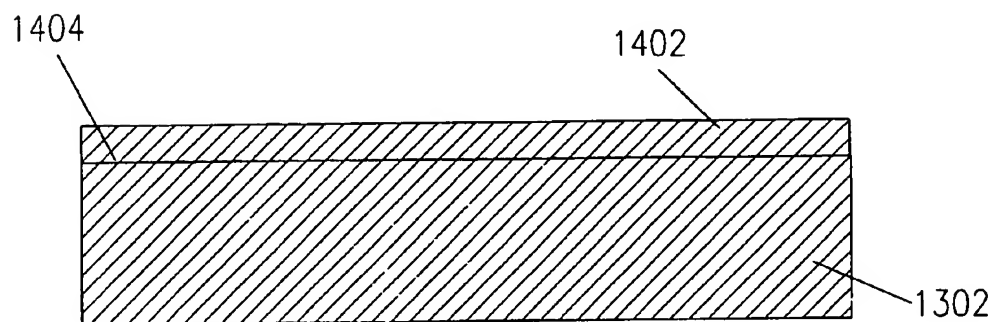
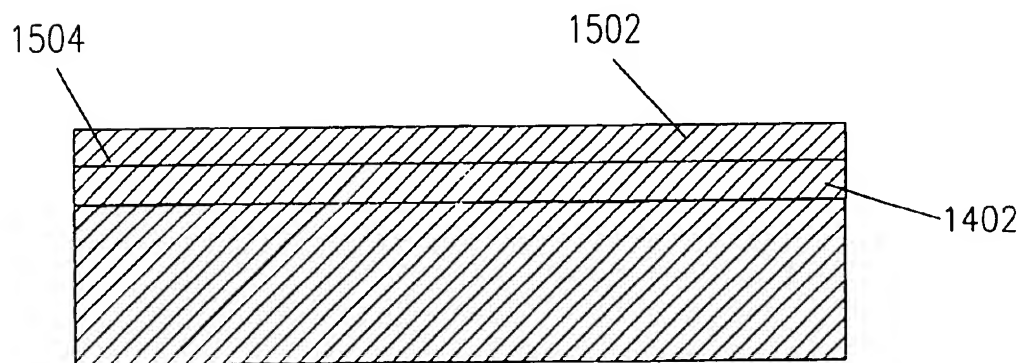


FIG. 12

**FIG. 13****FIG. 14****FIG. 15**

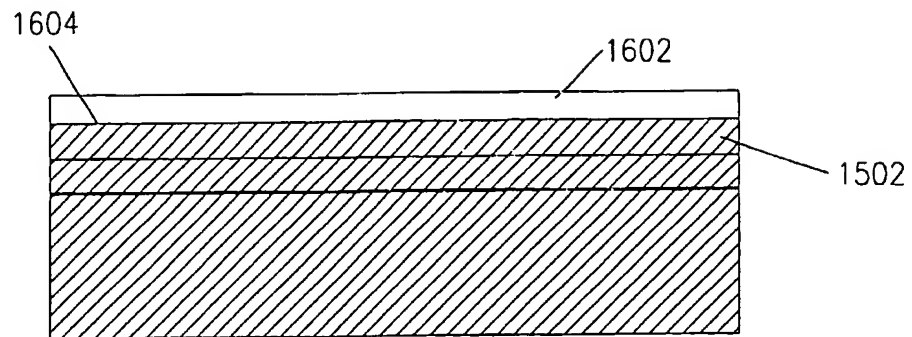


FIG. 16

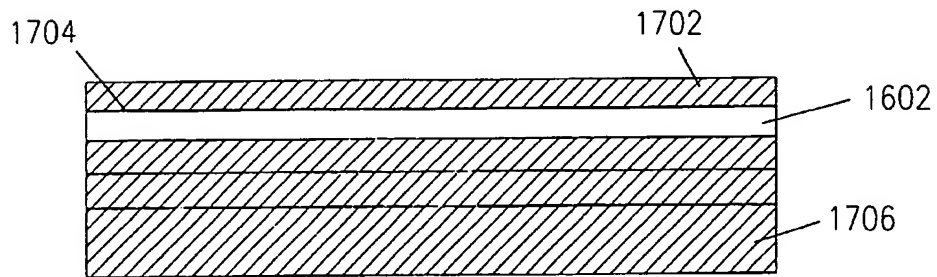


FIG. 17

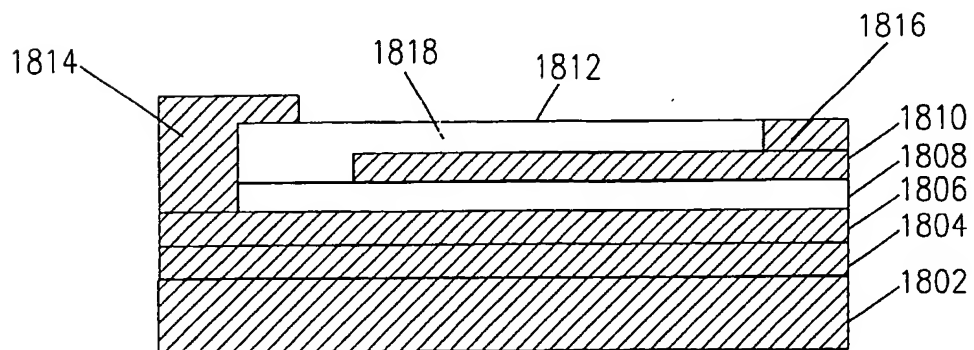


FIG. 18

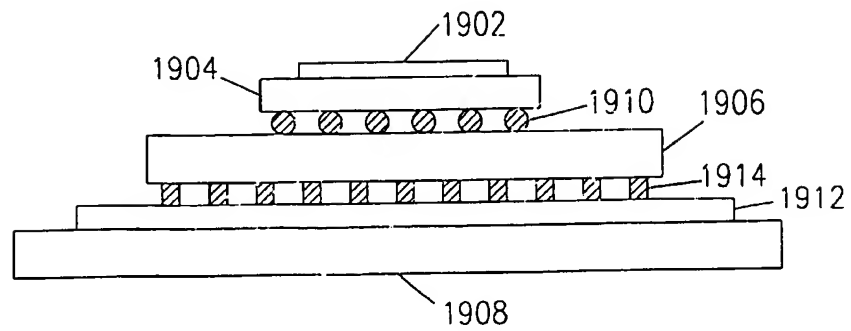


FIG. 19

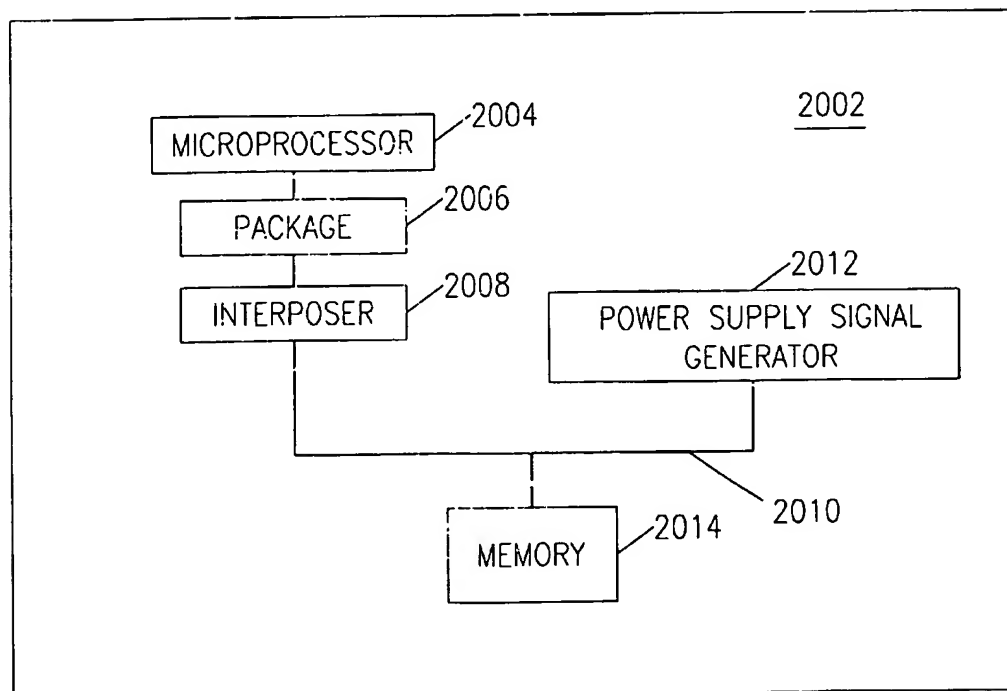


FIG. 20

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ELECTRONIC PACKAGE HAVING EMBEDDED CAPACITORS AND METHOD OF FABRICATION THEREFOR

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to apparatus for providing capacitance to an electronic circuit, and more particularly to embedded capacitors in an integrated circuit package, and methods of capacitor and package fabrication.

BACKGROUND OF THE INVENTION

Electronic circuits, and particularly computer and instrumentation circuits, have in recent years become increasingly powerful and fast. As circuit frequencies continue to escalate, with their associated high frequency transients, noise in the power and ground lines increasingly becomes a problem. This noise can arise due to inductive and capacitive parasitics, for example, as is well known. To reduce such noise, capacitors known as decoupling capacitors are often used to provide a stable signal or stable supply of power to the circuitry.

Capacitors are further utilized to dampen power overshoot when an electronic device (e.g., a processor) is powered up, and to dampen power droop when the device begins using power. For example, a processor that begins performing a calculation may rapidly need more current than can be supplied by the on-chip capacitance. In order to provide such capacitance and to dampen the power droop associated with the increased load, off-chip capacitance should be available to respond to the current need within a sufficient amount of time. If insufficient voltage is available to the processor, or if the response time of the capacitance is too slow, the die voltage may collapse. The localized portions of a die that require large amounts of current in short periods of time are often referred to as die "hot spots."

Decoupling capacitors and capacitors for dampening power overshoot or droop are generally placed as close as practical to a die load or hot spot in order to increase the capacitors' effectiveness. Often, the decoupling capacitors are surface mounted to the die side or land side of the package upon which the die is mounted. FIG. 1 illustrates a cross-section of an integrated circuit package 102 having die side capacitors 106 and land side capacitors 108 in accordance with the prior art. Die side capacitors 106, as their name implies, are mounted on the same side of the package as the integrated circuit die 104. In contrast, land side capacitors 108 are mounted on the opposite side of the package 102 as the die 104.

FIG. 2 illustrates an electrical circuit that simulates the electrical characteristics of the capacitors illustrated in FIG. 1. The circuit shows a die load 202, which may require capacitance or noise dampening in order to function properly. Some of the capacitance can be supplied by capacitance 204 located on the die. Other capacitance, however, must be provided off chip, as indicated by off-chip capacitor 206. The off-chip capacitor 206 could be, for example, the die side capacitors 106 and/or land side capacitors 108 illustrated in FIG. 1. The off-chip capacitor 206 may more accurately be modeled as a capacitor in series with some resistance and inductance. For ease of illustration, however, off-chip capacitance 206 is modeled as a simple capacitor.

Naturally, the off-chip capacitor 206 would be located some distance, however small, from the die load 202, due to manufacturing constraints. Accordingly, some inductance 208 exists between the die load and the off-chip capacitance. Because the inductance 208 tends to slow the response time

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of the off-chip capacitor 206, it is desirable to minimize the electrical distance between the off-chip capacitance 206 and the die load 202, thus reducing the inductance value 208. This can be achieved by placing the off-chip capacitor 206 as electrically close as possible to the die load.

Referring back to FIG. 1, die side capacitors 106 are mounted around the perimeter of the die 104, and provide capacitance to various points on the die through traces and vias (not shown) and planes in the package 102. Because die side capacitors 106 are mounted around the perimeter of the die, the path length between a hot spot and a capacitor 106 may result in a relatively high inductance feature between the hot spot and the capacitor 106.

In contrast, land side capacitors 108 can be mounted directly below die 104, and thus directly below some die hot spots. Thus, in some cases, land side capacitors 108 can be placed electrically closer to the die hot spots than can die side capacitors 106, resulting in a lower inductance path to between the die hot spot and the capacitance 108. However, the package also includes connectors (not shown), such as pins or lands, located on its land side. In some cases, placement of land side capacitors 108 on the package's land side would interfere with these connectors. Thus, the use of land side capacitors 108 is not always an acceptable solution to the inductance problem.

Besides the inductance issues described above, additional issues are raised by the industry's trend to continuously reduce device sizes and packing densities. Because of this trend, the amount of package real estate available to surface-mounted capacitors is becoming smaller and smaller.

As electronic devices continue to advance, there is an increasing need for higher levels of capacitance at reduced inductance levels for decoupling, power dampening, and supplying charge. In addition, there is a need for capacitance solutions that do not interfere with package connectors, and which do not limit the industry to certain device sizes and packing densities. Accordingly, there is a need in the art for alternative capacitance solutions in the fabrication and operation of electronic devices and their packages.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 illustrates a cross-section of an integrated circuit package having die side and land side capacitors in accordance with the prior art;

FIG. 2 illustrates an electrical circuit that simulates the electrical characteristics of the capacitors illustrated in FIG. 1;

FIG. 3 illustrates a cross-section of an electronic package including a set of embedded capacitors in accordance with one embodiment of the present invention;

FIG. 4 illustrates a flowchart of a method for fabricating an electronic package including embedded capacitors in accordance with one embodiment of the present invention;

FIGS. 5-9 are schematic cross-sections illustrating various stages of fabricating an electronic package including embedded capacitors in accordance with one embodiment of the present invention;

FIG. 10 illustrates a cross-section of an electronic package including an embedded capacitor in accordance with one embodiment of the present invention;

FIG. 11 illustrates a cross-section of an electronic package including a set of embedded capacitors in accordance with another embodiment of the present invention;

FIG. 12 illustrates a flowchart of a method for fabricating an integrated circuit capacitor in accordance with one embodiment of the present invention;

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FIGS. 13-17 are schematic cross-sections illustrating various stages of fabricating an integrated circuit capacitor in accordance with one embodiment of the present invention;

FIG. 18 illustrates a cross-section of an integrated circuit capacitor in accordance with another embodiment of the present invention;

FIG. 19 illustrates an integrated circuit package, interposer, and printed circuit board, each of which could include one or more embedded capacitors in accordance with various embodiments of the present invention; and

FIG. 20 illustrates a general purpose computer system in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Various embodiments of the present invention provide an electronic package that includes one or more embedded capacitors. The various embodiments could be implemented in a number of different types of electronic packages, including an integrated circuit package, a printed circuit board or an interposer (i.e., a circuit board that provides a dimensional interface between an integrated circuit package and a printed circuit board). The embodiments of the present invention provide a capacitance solution that effectively suppresses noise, dampens power overshoot and droop, and supplies charge to die hot spots in a timely manner.

In one embodiment, one or more capacitors are embedded within a device package and electrically connected to one or more die loads. The embedded capacitors are integrated circuit capacitors, in one embodiment. In another embodiment, the embedded capacitors are high dielectric ceramic capacitors. Because these capacitors are embedded within the device package, they do not interfere with connections on the package's land side. In addition, the capacitors can be embedded within the package at locations that are very close, electrically, to the various die loads.

FIG. 3 illustrates a cross-section of an electronic package 302 that includes a set of embedded capacitors 308, in accordance with one embodiment of the present invention. Package 302 includes a first layer 304, having a conductive material 306 deposited on its top surface. Mounted on the top surface are one or more embedded capacitors 308. A first terminal (not shown) of each of the one or more capacitors 308 makes electrical contact with the conductive material 306. A nonconductive layer 310 is deposited over the conductive material 306 and the one or more capacitors 308. Connections 312 electrically connect a second terminal (not shown) of each of the one or more capacitors 308 to a top surface of the nonconductive layer 310. The first and second terminals are electrically connected to an integrated circuit 314 through conductive pads 316 on the top surface of the package.

In the embodiment shown, the package is electrically connected to a printed circuit board 318 using solder ball connections 320, and the integrated circuit 314 is electrically connected to the top surface of the package using other solder ball connections 322. In another embodiment, the package could be mounted to the printed circuit board 318 using pins or other connectors. In addition, the integrated circuit 314 could be mounted to the package using wirebond technology or some other mounting technology.

The electronic package 302 shown in FIG. 3 is an integrated circuit package. In other embodiments, the embedded capacitor structure could be used in a printed circuit board and/or an interposer.

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FIG. 4 illustrates a flowchart of a method for fabricating an electronic package that includes embedded capacitors in accordance with one embodiment of the present invention. FIG. 4 should be viewed in conjunction with FIGS. 5-9, which are schematic cross-sections illustrating various stages of fabricating an electronic package including embedded capacitors in accordance with one embodiment of the present invention.

The method begins by performing two separable processes. The first process, represented by block 402, is to fabricate one or more capacitors that will be embedded within the electronic package. In one embodiment, one or more of the embedded capacitors are integrated circuit capacitors or, more specifically, planar chip capacitors on a silicon substrate. A method of making the planar chip capacitors, in accordance with various embodiments of the invention, is described in detail below in conjunction with FIGS. 12-18. In other embodiments, one or more of the embedded capacitors could be ceramic capacitors or other types of discrete capacitors. Methods of making the capacitors in accordance with these other embodiments are well known to those of skill in the art.

The second separable process, represented by blocks 404, 406, and 408, is to fabricate a first layer of the electronic package, which includes a conductive material deposited on its top surface. The term "first layer" is used for descriptive purposes herein, and is meant to include a single package level (e.g., a single conductive or non-conductive level) or multiple package levels formed during a build-up process. Fabricating the first layer includes at least three processes, as described in conjunction with blocks 404-408.

First, one or more levels of the electronic package are formed, in block 404, using package build-up processes well known to those of skill in the art. These processes can include, for example, any combination of photolithography, material deposition, plating, drilling, printing, lamination, and other processes for selectively adding or removing conductive and non-conductive materials.

In one embodiment, the one or more levels of the electronic package includes one or more levels of an organic substrate, such as an epoxy material, and one or more levels of patterned conductive material. If an organic substrate is used, for example, standard printed circuit board materials such as FR-4 epoxy-glass, polyimide-glass, benzocyclobutene, Teflon, other epoxy resins, or the like could be used in various embodiments. In alternate embodiments, the package could include an inorganic substance, such as ceramic, for example. In various embodiments, the thickness of the one or more levels is within a range of about 10-1000 microns, where each level is within a range of about 10-40 microns thick in one embodiment. The one or more levels could be thicker or thinner than these ranges in other embodiments.

Fabricating the first layer also includes forming one or more plated through hole (PTH) vias through one or more levels of the first layer, in block 406. Electronic packages commonly include multiple interconnect levels. In such a package, patterned conductive material on one interconnect level is electrically insulated from patterned conductive material on another interconnect level by dielectric material layers. Connections between the conductive material at the various interconnect levels are made by forming openings, referred to as vias, in the insulating layers and providing an electrically conductive structure such that the patterned conductive material from different interconnect levels are brought into electrical contact with each other. Coupled with

the electrically conductive structure, the vias are referred to as PTH vias. These structures can extend through one or more of the interconnect levels.

In various embodiments, the diameter of each via is within a range of about 50–300 microns. In addition, the length of each via could be in a range of about 10–1000 microns, depending on how many levels each via extends through. The diameters and lengths of vias could be larger or smaller than these ranges in other embodiments.

Vias could be through holes (i.e., holes through all levels of the first layer), or each via could be bounded above and/or below by various levels of the first layer. A via bounded on only one end is often termed a blind via, and a via bounded on both ends is often termed a buried via.

In one embodiment, vias are mechanically drilled and filled with a conductive material, although vias may also be punched, laser drilled, or formed using other techniques in various other embodiments. If the first layer is an inorganic substance, such as ceramic, other hole formation techniques known to those of skill in the art would be used. For example, the first layer could be created with vias already existing therein.

In one embodiment, some of these PTH vias are used to electrically connect one or both terminals of an embedded capacitor to one or more other layers of the package, as will be described below. In other embodiments, one or both terminals of the embedded capacitor are electrically connected to other layers of the package by forming electrical connections above the capacitor, as will be described below in conjunction with block 416.

Forming the first layer also includes forming a patterned conductive material level on the top surface of the first layer, in block 408. This formation process also could be used to plate or fill the vias, although they could be plated or filled in a separate process as well.

In one embodiment, the conductive material level is a copper layer, although other conductive metals such as tin, lead, nickel, gold, and palladium, or other materials could be used in other embodiments. In various embodiments, the thickness of conductive level is within a range of about 5–15 microns. The conductive level could be thicker or thinner than that range in other embodiments.

In one embodiment, the conductive level is formed using standard techniques for forming a conductive level. In one embodiment, the conductive level is formed by depositing a seed layer, such as sputter-deposited or electroless-deposited copper, on the top surface of the package, followed by electrolytic plating a layer of copper on the seed layer. In another embodiment, the conductive level is formed using standard photolithographic techniques. Other methods of depositing the conductive level will be apparent to those skilled in the art, such as screen printing or other printing of conductive inks. In still another embodiment, rather than using a package layer without a conductive material on its top surface, a clad laminate, such as a copper-clad laminate, could be used.

FIG. 5 illustrates a cross-section of a portion of an electronic package resulting from blocks 404–408, in accordance with one embodiment of the present invention. The portion of the electronic package includes a first non-conductive level 502, PTH via 504, and patterned conductive material level 506. Patterned conductive material level 506 includes conductive portions 508 and non-conductive portions 510. Conductive portions 508 include conductive traces and/or planes of conductive material. In one embodiment, at least a part of conductive portions 508 is

electrically connected to PTH via 504. Thus, part of conductive portion 508 makes electrical contact with one or more other levels of the electronic package.

As mentioned previously, first level 502 is a non-conductive material, in one embodiment. In an alternate embodiment, first level 502 could be a conductive material, and PTH via 504 would be structurally modified to have an inner and outer conductor, as is known by those of skill in the art. The outer conductor could be formed by the first conductive level, and the inner conductor and outer conductor would be electrically isolated.

Referring back to FIG. 4, one or more of the capacitors fabricated in block 402 are mounted on the top surface of the first layer in block 410. In various embodiments, the capacitors could be planar chip capacitors, ceramic capacitors, or some other type of discrete capacitor, as described previously. As illustrated in FIG. 6, in one embodiment, each capacitor 602 is mounted so that a first terminal 604 of the capacitor makes electrical contact with a conductive portion 508 of the patterned conductive material level 506.

In one embodiment, the first terminal 604 is located along a bottom surface of capacitor 602, and a second terminal 606 is located along a top surface. In other embodiments, the first or second terminals could be along a side and/or top surface of capacitor 602, and/or capacitor 602 could have multiple contacts that form a single terminal. Most capacitor structures include the equivalent of two conductive surfaces separated by a dielectric, and the term “terminal,” as used herein, means one or more contacts on the capacitor package that electrically connect to one of the two conductive surfaces within the interior capacitor structure.

Capacitor 602 is mounted to the top surface of the first layer, in one embodiment, by attaching capacitor 602 to the top surface using a conductive adhesive film or paste (not shown). In other embodiments, where the capacitor's terminal is not along the bottom of the capacitor 602, a non-conductive film or paste could be used. If an adhesive film is used, it is cut and attached to the first layer at locations where the capacitors 602 are to be placed. Similarly, if a paste is used, it is screen printed at the capacitor locations, in one embodiment. Alternatively, the adhesive film or paste could be applied to the capacitor 602 before it is applied to the first layer.

In still other embodiments, the capacitor 602 could be attached to the top surface with one or more solder connections (not shown). Although capacitor 602 is shown to be mounted over a conductive portion of the first layer, capacitor 602 could be mounted over a non-conductive portion of the first layer in an alternate embodiment.

Although only a single capacitor 602 is shown mounted on the first layer, more capacitors (not shown) also could be mounted on the first layer. In addition, as will be described later, one or more capacitors could be mounted to other package layers (not shown) as well.

Referring back to FIG. 4, a non-conductive layer of material is applied, in block 412, on the top surface and over the one or more capacitors. FIG. 7 illustrates non-conductive layer 702 applied over the top surface of the first layer and over capacitor 602. In one embodiment, the thickness of non-conductive layer 702 is in a range of about 80–150 microns. Layer 702 could have a thickness outside of this range in other embodiments. Also, in one embodiment, the non-conductive layer has a dielectric constant in a range of 4–5. In other embodiments, the layer could have a larger or smaller dielectric constant.

In one embodiment, a liquid, photoimageable film is screen-printed over the top surface, cured, and photoimaged

to form non-conductive layer 702. In another embodiment, non-conductive layer 702 includes one or more sheets of dry film that are vacuum laminated over the top surface and cured. Depending on the thickness of each sheet of non-conductive film, the number of sheets applied over the top surface could be in a range of about 1–20 sheets. In other embodiments, the number of sheets could be larger than this range.

In some cases, application of the non-conductive layer 702 could result in a bump (not shown) in the top surface 704 of the non-conductive layer 702 over the capacitor 602. This condition is less likely when a non-conductive liquid is used to form the non-conductive layer 702, since a sufficiently viscous liquid is self-planarizing.

Referring back to FIG. 4, the top surface 704 of the non-conductive layer 702 is planarized, in block 414, if necessary. Planarization could be performed, for example, by pressing, mechanically grinding, and/or polishing the top surface until it is sufficiently smooth.

In block 416, the second terminal 606 of the capacitor 602 is electrically connected to the top surface 704 of the non-conductive layer 702. In one embodiment, as illustrated in FIG. 8, this is done by forming one or more contact holes 802 through the top surface 704 and extending to the second terminal 606. Forming contact holes 802 could be done, for example, by mechanically or laser drilling contact holes 802 or using a photolithography process. In alternate embodiments, terminals 606 could be formed using other techniques, such as laser ablation, imprinting, perforation, or other less-common or developing techniques. In one embodiment, contact holes 802 have a diameter in a range of about 50–300 microns. Larger or smaller diameter contact holes 802 could be used in other embodiments.

In one embodiment, the second terminal is located on the top of capacitor 602, and thus contact holes 802 would form openings to the top of capacitor 602. In other embodiments, the second terminal could be located on or towards the sides and/or bottom of capacitor 602, and contact holes 802 would be located accordingly.

In order to electrically connect the second terminal to the top surface 704, additional conductive material is deposited into contact holes 802. As illustrated in FIG. 9, the conductive material 902 within the contact holes is electrically connected to an additional layer of patterned conductive material 904. This facilitates the electrical connection of the second terminal 606 to the top surface and beyond.

Referring back to FIG. 4, the build up process continues, if appropriate, in block 418. Thus, using techniques known to those of skill in the art, one or more additional package layers (not shown) of conductive and non-conductive materials can be deposited over conductive material layer 904. The number of additional layers, if any, that are built up depends on the package design. During the build up process, the first and second terminals of the capacitor continue to be electrically connected to the top surface of the package.

In one embodiment, part of the build up process includes mounting, embedding, and electrically connecting one or more additional capacitors within one or more additional layers of the package. Thus, embedded capacitors could be located within one or more layers of the package. After the build up process is completed, the method ends.

FIG. 10 illustrates a cross-section of an electronic package including an embedded capacitor in accordance with one embodiment of the present invention. In the embodiment shown, the package is an integrated circuit package, upon which an integrated circuit 1002 is mounted.

One or more loads (not shown) within integrated circuit 1002 are electrically connected to embedded capacitor 1004. The first terminal 1006 of capacitor 1004 is connected to the load(s) via electrical connections 1008, 1009, 1010, 1011, and solder bump 1012. The second terminal 1014 is connected to the load via electrical connections 1016, 1017, 1018, and solder bump 1012.

In addition, during operation, the first terminal 1006 is coupled to a first potential source, and the second terminal 1014 is coupled to a second potential source. For example, the first and second potential sources can be a ground potential and a supply potential, Vcc. Which terminal is coupled to which potential source is a matter of design, as either set can be connected to either source.

As shown in FIG. 10, electrical connections 1008–1011 and 1016–1018 can be formed by one or more vias and/or conductive traces. FIG. 10 is for illustrative purposes only, and numerous different configurations for electrically connecting the terminals 1006, 1014 of capacitor 1004 to the top surface 1020 of the package could be used. In particular, the number of package layers between the capacitor 1004 and the top surface 1020 could be different, the location of the capacitor's terminals could be different, and the locations and numbers of the constituent parts of electrical connections 1008–1011 and 1016–1018 could be different than shown.

In one embodiment, at least some of the embedded capacitors 1004 are disposed underneath the integrated circuit 1002. The embedded capacitors 1004 may be dispersed evenly underneath the integrated circuit 1002, or concentrations of embedded capacitors 1004 could be provided to produce additional capacitance for the die hot spots. Although only a single capacitor 1004 is illustrated in FIG. 10, in practice, many more embedded capacitors could be dispersed underneath the integrated circuit 1002 in order to provide sufficient capacitance. In alternate embodiments, some or all of the embedded capacitors 1004 are located in areas of the package that are not underneath integrated circuit 1002.

As mentioned previously, capacitors could be embedded within multiple different layers of a package, in various embodiments. FIG. 11 illustrates a cross-section of an electronic package including a set of embedded capacitors in accordance with another embodiment of the present invention. Capacitor 1102 is embedded within a first layer 1104 of the package, and capacitor 1106 is embedded within a second layer 1008 of the package. Electrical connections are made between the capacitors' terminals and the top surface of the package, to which an integrated circuit 1110 is electrically connected.

Implementation of the embedded capacitor structure in an integrated circuit package is just one embodiment of the present invention. In another embodiment, the embedded capacitor structure is implemented in a printed circuit board. In that embodiment, a socket, pads or some other connectors are located on the top surface of the package and interconnected to the embedded capacitors. In still another embodiment, the embedded capacitor structure is implemented in an interposer. When used in an interposer, the top surface of the package also includes a socket, pads or some other connectors that are electrically coupled to the embedded capacitors.

As described previously, various types of capacitors can be embedded within an electronic package in various embodiments. In one embodiment, an "integrated circuit capacitor," is used. The integrated circuit capacitor can be

formed on a silicon substrate or some other type of substrate, in various embodiments.

As mentioned previously, many capacitor structures include the equivalent of two conductive surfaces separated by a dielectric. In one embodiment, the integrated circuit capacitor includes two or more electrodes and $N-1$ thin film dielectric layers, where N is the number of electrodes present. Thus, in the embodiment described below having two electrodes, a single thin film dielectric layer is used.

FIG. 12 corresponds to block 402 (FIG. 4), and illustrates a flowchart of a method for fabricating an integrated circuit capacitor in accordance with one embodiment of the present invention. FIG. 12 should be viewed in conjunction with FIGS. 13-17, which are schematic cross-sections illustrating various stages of fabricating an integrated circuit capacitor in accordance with one embodiment of the present invention.

The method begins, in block 1202, by fabricating a silicon substrate. FIG. 13 illustrates a cross-section of a portion of a silicon substrate 1302 in accordance with one embodiment of the present invention. In other embodiments, substrates composed of materials other than silicon can be used.

In one embodiment, silicon substrate 1302 is a highly doped, $n+$ silicon wafer having a resistivity of less than 0.1 Ohms/centimeter. As such, silicon substrate 1302 is conductive and forms a portion of a bottom terminal of a silicon chip capacitor. In an alternate embodiment, an n or p type silicon wafer could be used having a resistivity of less than 50 Ohms/centimeter. In another alternate embodiment, the silicon substrate 1302 is not used as part of the bottom terminal. Instead, connectivity to the electrode (described in conjunction with blocks 1204 and 1206) is provided through vias. In such an embodiment, the resistivity of the substrate 1302 is not as important.

Another portion of the bottom terminal is formed by depositing a barrier layer, in block 1204, on the silicon substrate. FIG. 14 illustrates barrier layer 1402 deposited on the top surface 1404 of silicon substrate 1302.

In one embodiment, the barrier layer is made of a highly doped, conductive substrate material having a low sheet resistivity. For example, materials such as titanium or titanium nitride could be used. The barrier layer is deposited on the silicon substrate using deposition techniques well known to those of skill in the art. In one embodiment, barrier layer 1402 has a thickness in a range of about 100-1000 Angstroms. A layer having a thickness that is greater or smaller than the above range can be used in other embodiments.

Referring back to FIG. 12, a bottom electrode is deposited on the barrier layer, in block 1206, using deposition techniques well known to those of skill in the art. FIG. 15 illustrates bottom electrode 1502 deposited on the top surface 1504 of barrier layer 1402, in accordance with one embodiment of the present invention.

Bottom electrode 1502 completes a bottom terminal of the silicon chip capacitor. In one embodiment, the bottom electrode is made of a material that is compatible with the capacitor's dielectric layer (described below). For example, materials such as platinum, palladium, tungsten, or AlSiCu could be used. In other embodiments, other conductive materials could be used. In one embodiment, bottom electrode 1502 has a thickness in a range of about 1-10 microns. An electrode having a thickness that is greater or smaller than the above range can be used in other embodiments.

Next, in block 1208, a dielectric layer is deposited on the bottom electrode. FIG. 16 illustrates dielectric layer 1602 deposited on the top surface 1604 of the bottom electrode 1502, in accordance with one embodiment of the present invention.

In one embodiment, the dielectric layer is a high-dielectric ferroelectric in the perovskite structure, such as SrTiO_3 , BaTiO_3 , $\text{Pb}(\text{Zr})\text{TiO}_3$, or other high dielectric constant materials, such as Ta_2O_5 . The dielectric layer is deposited on the bottom electrode using deposition techniques well known to those of skill in the art. In one embodiment, dielectric layer has a thickness in a range of about 100-1000 Angstroms. A layer having a thickness that is greater or smaller than the above range can be used in other embodiments.

In one embodiment, dielectric layer 1602 has a relatively high dielectric constant (e.g., in a range of about 2000 to 5000 or more). In this manner, the capacitor provides a relatively large amount of charge, when needed. In alternate embodiments, dielectric layer 1602 could have a dielectric constant that is higher or lower than the above range.

Referring again to FIG. 12, a top electrode is deposited on the dielectric layer in block 1210. FIG. 17 illustrates top electrode 1702 deposited on the top surface 1704 of dielectric layer 1602, in accordance with one embodiment of the present invention.

In one embodiment, the top electrode 1702 is made of the same material using the same deposition techniques as described in conjunction with depositing the bottom electrode, in block 1206. In addition, the top electrode 1702 has about the same thickness as the bottom electrode. In other embodiments, the material, deposition technique, and/or electrode thickness can be different for the top and bottom electrodes.

After depositing the top electrode 1702, the capacitor structure is complete. Next, in one embodiment, the bottom surface of the silicon substrate is back grinded, in block 1212. This is done in order to reduce the thickness of the substrate, as illustrated by a thinner silicon substrate 1706 in FIG. 17. Back grinding is performed, in one embodiment, by mechanically grinding or polishing the bottom surface of the silicon substrate.

Finally, in block 1214, multiple capacitors are singulated by dicing the structure into pieces. Singulating the capacitors is performed, in one embodiment, by laser or mechanical sawing. Other singulation techniques well known to those of skill in the art can be used in other embodiments. In an alternate embodiment, a "dice before grind" process could be used, where the process of singulating the capacitors (block 1214) occurs before back grinding (block 1212).

Each of the singulated capacitors has a thickness in a range of about 30-150 microns, and a depth and width in a range of about 5-10 millimeters, in one embodiment. In other embodiments, the dimensions of each capacitor can be larger or smaller than the above ranges. After singulating the capacitors, the method ends.

FIG. 17 illustrates a simple capacitive structure having a first terminal (formed from the bottom electrode, the barrier layer, and the silicon substrate), a dielectric layer, and a top electrode that forms the second terminal. As will be obvious to one of skill in the art based on the description herein, the capacitive structure can be modified into various configurations while still achieving the same purpose. For example, FIG. 18 illustrates a cross-section of an integrated circuit capacitor in accordance with another embodiment of the present invention.

The capacitor shown in FIG. 18 also includes a thinned silicon substrate 1802, a barrier layer 1804, a bottom electrode 1806, a dielectric layer 1808, and a top electrode 1810. Unlike the capacitor of FIG. 17, however, both electrodes 1806, 1810 of the capacitor of FIG. 18 are electrically

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connected to the top surface 1812 of the capacitor. The top connections are made, in one embodiment, using connectors 1814 and 1816 to electrically connect the bottom and top electrodes 1806, 1810, respectively, to the top surface 1812. In addition, an additional dielectric layer 1818 is used to electrically isolate connectors 1814 and 1816.

Although many of the same deposition, back grinding, and singulation techniques can be used to fabricate the capacitor of FIG. 18, additional steps are also necessary to form and isolate connectors 1814 and 1816. For example, after the top electrode 1810 is formed, portions of the top electrode are selectively removed, and an additional dielectric layer 1818 is deposited on the top surface of the top electrode 1810.

Then, portions of dielectric layers 1818 and 1808 are selectively removed to expose portions of the top and bottom electrodes 1810, 1806. Standard silicon via or plug processing techniques are then employed, in one embodiment, to form connectors 1814 and 1816. Other techniques well known to those of skill in the art also could be employed in other embodiments.

The capacitor shown in FIG. 18 is a single-layer capacitor. In other embodiments, portions of the build up process could be repeated in order to form a multi-layer capacitor. In such embodiments, additional conductive and non-conductive layers would be built up on the top surface 1812 of dielectric layer 1818, essentially forming multiple capacitors that are capable of holding a greater amount of charge.

As described previously, one or more of the capacitors illustrated in FIGS. 17 and 18, or other appropriate substitutes, are embedded within an integrated circuit package, interposer, and/or printed circuit board. FIG. 19 illustrates an integrated circuit package 1904, interposer 1906, and printed circuit board 1908, each of which could include one or more embedded capacitors in accordance with various embodiments of the present invention.

Starting from the top of FIG. 19, an integrated circuit 1902 is housed by integrated circuit package 1904. Integrated circuit 1902 contains one or more circuits which are electrically connected to integrated circuit package 1904 by connectors (not shown).

Integrated circuit 1902 could be any of a number of types of integrated circuits. In one embodiment of the present invention, integrated circuit 1902 is an microprocessor, although integrated circuit 1902 could be other types of devices in other embodiments. In the example shown, integrated circuit 1902 is a "flip chip" type of integrated circuit, meaning that the input/output terminations on the chip can occur at any point on its surface. After the chip has been readied for attachment to integrated circuit package 1904, it is flipped over and attached, via solder bumps or balls to matching pads on the top surface of integrated circuit package 1904. Alternatively, integrated circuit 1902 could be wire bonded, where input/output terminations are connected to integrated circuit package 1904 using bond wires to pads on the top surface of integrated circuit package 1904.

One or more of the circuits within integrated circuit 1902 acts as a load, which may require capacitance, noise suppression, and/or power dampening. Some of this capacitance is provided, in one embodiment of the present invention, by capacitors (not shown) embedded within integrated circuit package 1904.

In this manner, one or more levels of additional capacitance are provided to integrated circuit 1902, also providing power dampening and noise suppression, when needed. The close proximity of these off-chip sources of capacitance

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means that each source has a relatively low inductance path to the die. In other embodiments, the capacitors are embedded within the printed circuit board 1908, interposer 1906, or some combination thereof.

Integrated circuit package 1904 is coupled to interposer 1906 using solder connections, such as ball grid array connections 1910, for example. In another embodiment, integrated circuit package 1904 could be electrically and physically connected to interposer 1906 using a pinned connection, as described below.

Interposer 1906 is coupled to printed circuit board 1908 through a socket 1912 on printed circuit board 1908. In the example shown, interposer 1906 includes pins 1914, which mate with complementary pin holes in socket 1912. Alternatively, interposer 1906 could be electrically and physically connected to printed circuit board 1908 using solder connections, such as ball grid array connections, for example. In still another alternate embodiment, integrated circuit package 1904 could be connected directly to printed circuit board 1908, without using an interposer. In such an embodiment, integrated circuit package 1904 and printed circuit board 1908 could be electrically and physically connected using ball grid array or pinned connections. Other ways of connecting integrated circuit package 1904 and printed circuit board 1908 could also be used in other embodiments.

Printed circuit board 1908 could be, for example, a motherboard of a computer system. As such, it acts as a vehicle to supply power, ground, and other types of signals to integrated circuit 1902. These power, ground, and other signals are supplied through traces or planes (not shown) on or within printed circuit board 1908, socket 1912, pins 1914, and traces (not shown) on or within interposer 1906 and integrated circuit package 1904.

The package described above in conjunction with various embodiments could be a integrated circuit package, interposer, or printed circuit board forming part of a general purpose computer system. FIG. 20 illustrates a general purpose computer system in accordance with one embodiment of the present invention.

The computer system is housed on printed circuit board 2002, and includes microprocessor 2004, integrated circuit package 2006, interposer 2008, bus 2010, power supply signal generator 2012, and memory 2014. Integrated circuit package 2006, interposer 2008, and/or printed circuit board 2002 include one or more embedded capacitors in accordance with various embodiments of the present invention, described above. Integrated circuit package 2006 and interposer 2008 couple microprocessor 2004 to bus 2010 in order to deliver power and communication signals between microprocessor 2004 and devices coupled to bus 2010. For the embodiment of the present invention shown in FIG. 20, bus 2010 couples microprocessor 2004 to memory 2014 and power supply signal generator 2012. However, it is to be understood that in alternative embodiments of the present invention, microprocessor 2004 can be coupled to memory 2014 and power supply signal generator 2012 through two different busses.

CONCLUSION

Thus, various embodiments of an electronic package having one or more embedded capacitors and methods of fabricating that package have been described, along with a description of the incorporation of a package within a general purpose computer system. In addition, various embodiments relating to the fabrication of the package and capacitor have also been described.

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While the foregoing examples of dimensions and ranges are considered typical, the various embodiments of the invention are not limited to such dimensions or ranges. It is recognized that the trend within industry is to generally reduce device dimensions for the associated cost and performance benefits.

In the foregoing detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention.

It will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown.

For example, illustrative embodiments show capacitors embedded within certain layers of a package. However, those skilled in the art will recognize that the embedded capacitors could be included in one or more other layers, in accordance with the present invention. Also, besides having application in an integrated circuit package, the embedded capacitors can be used in place of various discrete components on an interposer or printed circuit board, in other embodiments. In addition, additional layers of patterned conductive materials and interconnects for carrying signals, power, and ground may exist between, above, or below the layers shown in the figures.

The various embodiments have been described in the context of providing excess, off-chip capacitance to a die. One of ordinary skill in the art would understand, based on the description herein, that the method and apparatus of the present invention could also be applied in many other applications where an embedded capacitor having a low inductance path to a circuit load are desired. Therefore, all such applications are intended to fall within the spirit and scope of the present invention.

This application is intended to cover any adaptations or variations of the present invention. The foregoing detailed description is, therefore, not to be taken in a limiting sense, and it will be readily understood by those skilled in the art that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated in order to explain the nature of this invention may be made without departing from the spirit and scope of the invention as expressed in the adjoining claims.

What is claimed is:

1. An electronic package comprising:
 - a first layer of the electronic package having a top surface; at least one discrete capacitor mounted on the top surface, wherein each of the at least one discrete capacitor has a first terminal and a second terminal;
 - a non-conductive layer applied on the top surface and over the at least one discrete capacitor; and electrical connections between the first terminal and the second terminal of the at least one discrete capacitor and a top surface of the non-conductive layer.
2. The electronic package as claimed in claim 1, wherein the electronic package is an integrated circuit package that is electrically connectable to an integrated circuit.
3. The electronic package as claimed in claim 1, wherein the electronic package is an interposer that is electrically connectable to an integrated circuit package.
4. The electronic package as claimed in claim 1, wherein the electronic package is a printed circuit board that is electrically connectable to an integrated circuit package.

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5. The electronic package as claimed in claim 1, wherein each of the at least one capacitor comprises:

- a bottom electrode, which forms at least a part of the first terminal;
- a dielectric layer connected to the bottom electrode; and
- a top electrode, connected to the dielectric layer, which forms at least a part of the second terminal, wherein the bottom electrode is formed on a silicon substrate.

6. The electronic package as claimed in claim 1, further comprising:

- one or more additional capacitors mounted on one or more additional layers of the electronic package.

7. A computer system positioned on a printed circuit board, the computer system comprising:

- a bus;
- a memory coupled to the bus; and
- an integrated circuit package coupled to the bus, including:

- an electronic package having a first layer with a top surface, at least one capacitor mounted on the top surface, wherein the capacitor has a first terminal and a second terminal, a non-conductive layer applied on the top surface and over the at least one capacitor, and electrical connections between the first terminal and the second terminal of the at least one capacitor and a top surface of the non-conductive layer, and
- a microprocessor located on a top surface of the electronic package, the microprocessor containing a circuit that is electrically connected to the first terminal and the second terminal.

8. The computer system as claimed in claim 7, further comprising:

- one or more additional capacitors mounted on one or more additional layers of the electronic package.

9. The computer system as claimed in claim 7, wherein each of the one or more capacitors comprises:

- a bottom electrode that forms at least a part of the first terminal;
- a dielectric layer connected to the bottom electrode; and
- a top electrode, connected to the dielectric layer, that forms at least a part of the second terminal, wherein the bottom electrode is formed on a silicon substrate.

10. A method for fabricating an electronic package, the method comprising:

- mounting a discrete capacitor on a top surface of a first layer of the electronic package, wherein the discrete capacitor has a first terminal and a second terminal;
- applying a non-conductive layer on the top surface and over the discrete capacitor; and
- electrically connecting the first terminal and the second terminal of the discrete capacitor to a top surface of the non-conductive layer.

11. The method as claimed in claim 1, further comprising: mounting one or more additional capacitors on the top surface of the first layer.

12. The method as claimed in claim 10, further comprising:

- mounting one or more additional capacitors on one or more other layers of the electronic package.

13. The method as claimed in claim 10, wherein mounting the capacitor comprises:

- attaching the capacitor to the top surface with an adhesive film.

14. The method as claimed in claim 10, wherein mounting the capacitor comprises:

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attaching the capacitor to the top surface with one or more solder connections.

15. The method as claimed in claim 10, wherein applying the non-conductive layer comprises:

laminating one or more sheets of non-conductive film on the top surface; and

curing the one or more sheets of non-conductive film.

16. The method as claimed in claim 15, further comprising:

planarizing the one or more sheets of non-conductive film.

17. The method as claimed in claim 1, wherein applying the non-conductive layer comprises:

screen-printing a photoimagable liquid on the top surface;

curing the photoimagable liquid; and

photoimaging the photoimagable liquid.

18. The method as claimed in claim 1, wherein applying the non-conductive layer comprises:

applying a non-conductive layer having a thickness in a range of about 80 to 150 microns.

19. The method as claimed in claim 1, wherein electrically connecting the second terminal comprises:

forming contact holes through the top surface of the non-conductive layer to the second terminal; and

depositing additional conductive material in the contact holes.

20. The method as claimed in claim 1, further comprising:

building up one or more additional package layers on the top surface of the electronic package; and

electrically connecting the first terminal and the second terminal to a top surface of the one or more additional package layers.

21. A method for fabricating an electronic package, the method comprising:

mounting a capacitor on a top surface of a first layer of the electronic package, wherein the capacitor has a first terminal and a second terminal, and wherein the capacitor includes a bottom electrode that forms at least a part of the first terminal, a dielectric layer, and a top electrode that forms at least a part of the second terminal, wherein the bottom electrode is formed on a silicon substrate;

applying a non-conductive layer on the top surface and over the capacitor; and

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electrically connecting the first terminal and the second terminal of the capacitor to a top surface of the non-conductive layer.

22. The method as claimed in claim 21, further comprising:

depositing a barrier layer on a silicon substrate;

depositing the bottom electrode on a top surface of the barrier layer;

depositing a dielectric layer on a top surface of the bottom electrode; and

depositing the top electrode on a top surface of the dielectric layer.

23. The method as claimed in claim 22, further comprising:

singulating the capacitor by separating the capacitor from multiple other capacitors deposited on the silicon substrate.

24. The method as claimed in claim 22, further comprising:

back grinding the silicon substrate to reduce a thickness of the silicon substrate.

25. The method as claimed in claim 22, wherein depositing the barrier layer comprises:

depositing a barrier layer having a thickness in a range of about 100 to 1000 Angstroms.

26. The method as claimed in claim 22, wherein depositing the barrier layer comprises:

depositing a barrier layer of a highly doped, conductive substrate material.

27. The method as claimed in claim 22, wherein depositing the bottom electrode comprises:

depositing a bottom electrode having a thickness in a range of about 1 to 10 microns.

28. The method as claimed in claim 22, wherein depositing the dielectric layer comprises:

depositing a dielectric layer having a thickness in a range of about 100 to 1000 Angstroms.

29. The method as claimed in claim 22, wherein depositing the top electrode comprises:

depositing a top electrode having a thickness in a range of about 1 to 10 microns.

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